

ISL74420 iSim Model User Guide

Introduction

This document serves as a description of the functions in the ISL74420 iSim model.

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1. Typical Evaluation Schematic Description

The typical application to evaluate this part is with CLKOUT0 and CLKOUT1 providing a 2MHz 2-phase clock, CLKOUT2 providing 1MHz and CLKOUT3 providing 500kHz.

Refer to Figure 1. Initially, the model is operating from its internal 48MHz oscillator. The period on CLKOUT2 (1MHz) is 1.000355us (3.897264-2.896909), which rounds out to 1.00MHz.

Partway through the simulation, we apply a 50MHz CLKIN that takes over from the internal oscillator. The CLKIN is the top trace. The period on CLKOUT2 changes to only 960ns, which equates to 1.041MHz. This is 4% faster than the nominal 1MHz so it shows that the core clock is 50MHz instead of 48MHz.

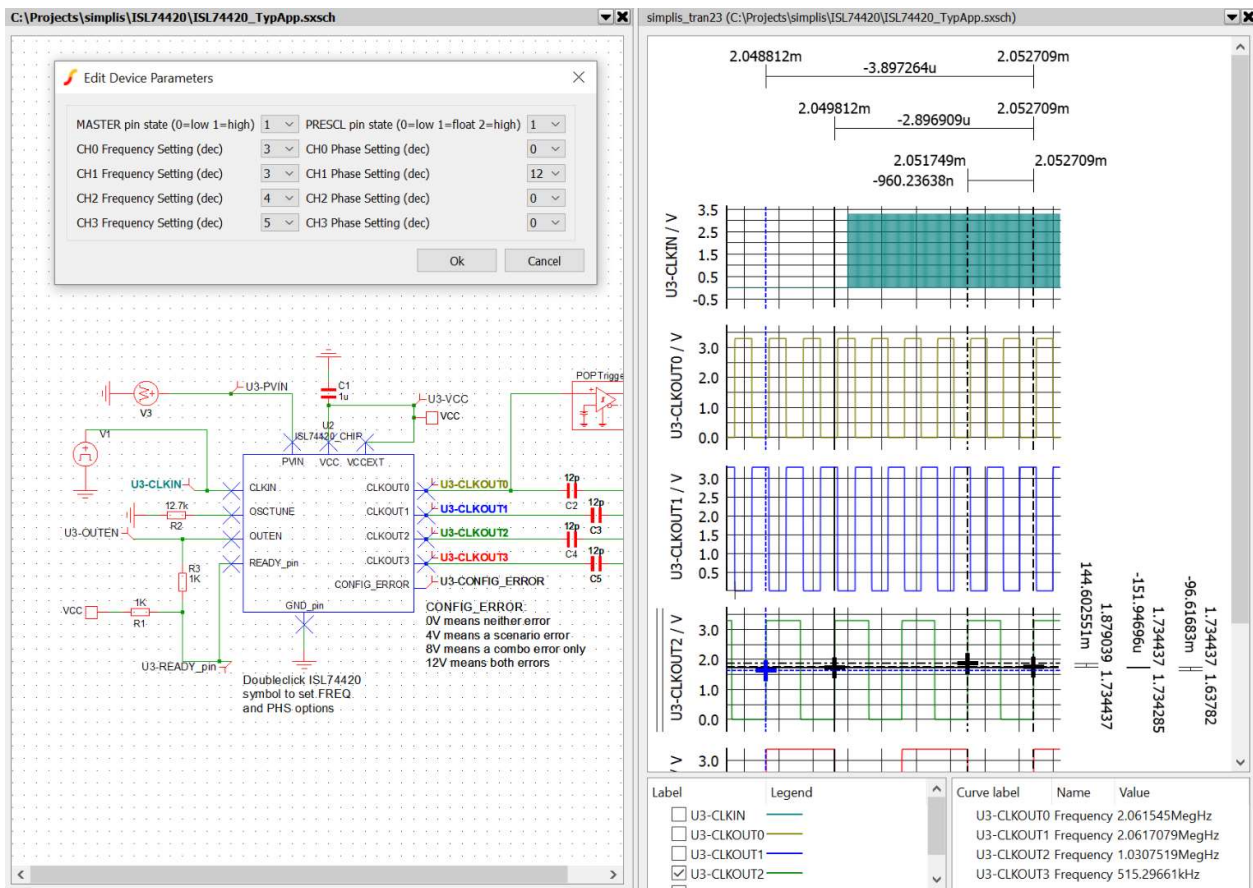


Figure 1: ISL74420 Typical Application

2. ISL74420 DEMO1Z Testbench

In the ISL74420_DEMO1Z application, all four outputs are configured for 2MHz with the PRESCL set low. The CLKOUT[0:3] phases are configured as 0°, 180°, 90°, and 270°. This configuration could be useful for a 2MHz 4-phase converter, or a 1MHz 8-phase converter if the controllers support dividing their CLKIN by 2.

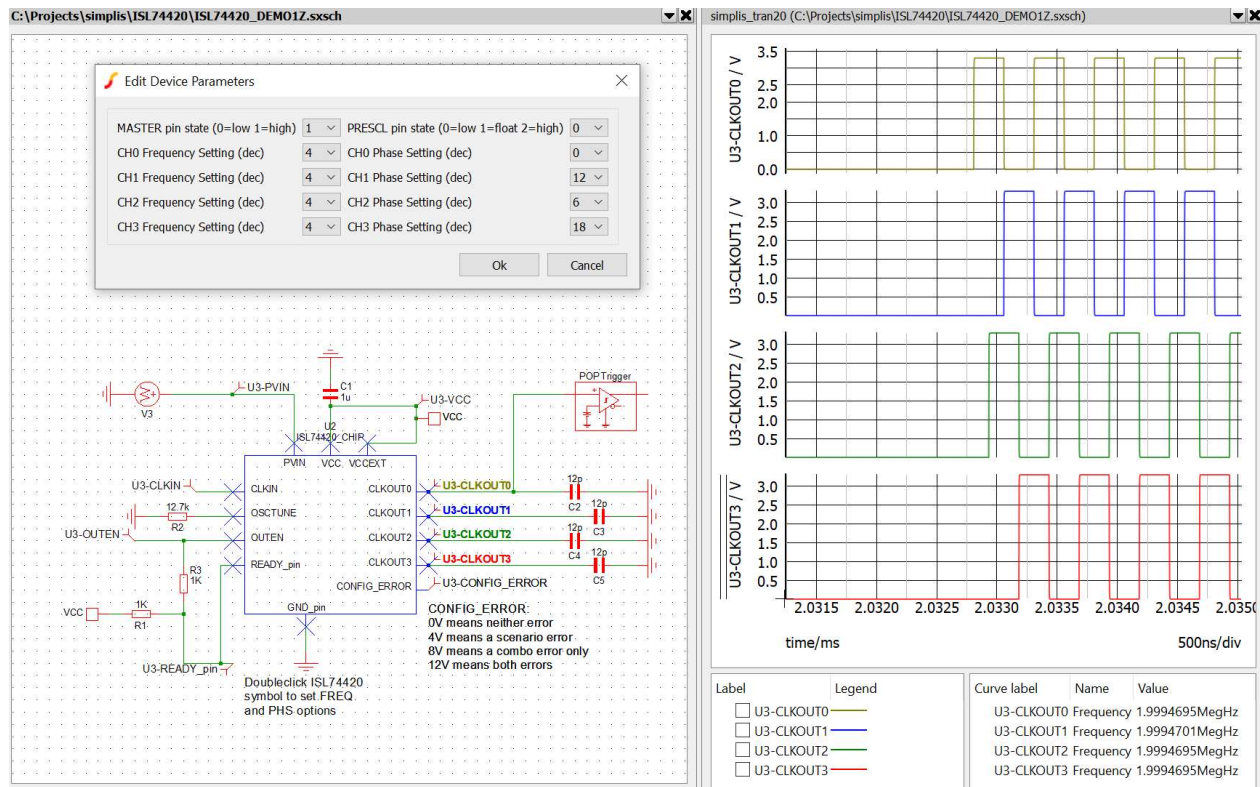


Figure 2: ISL74420_DEMO1Z testbench

3. Cascaded ISL74420 Schematic Description

An application schematic is included that replicates the settings needed for the ISLVERSALDEMO3Z board. The leader is set up for:

- CLKOUT0 500kHz 0d
- CLKOUT1 500kHz 180d
- CLKOUT2 1000kHz 0d
- CLKOUT3 6MHz 0d

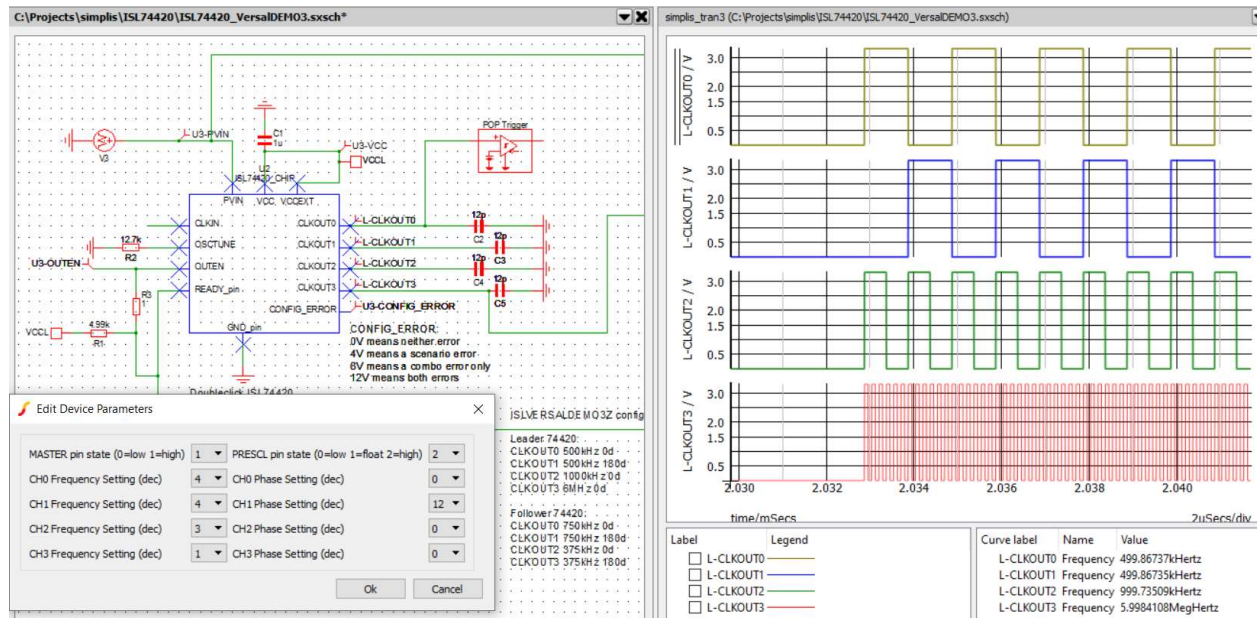


Figure 3: VERSALDEMO3 application: Leader settings and results

The follower is set up to match the follower settings in the VERSALDEMO3 application. The follower receives its CLKIN from the leader's CLKOUT3.

- CLKOUT0 750kHz 0d
- CLKOUT1 750kHz 180d
- CLKOUT2 375kHz 0d
- CLKOUT3 375kHz 180d

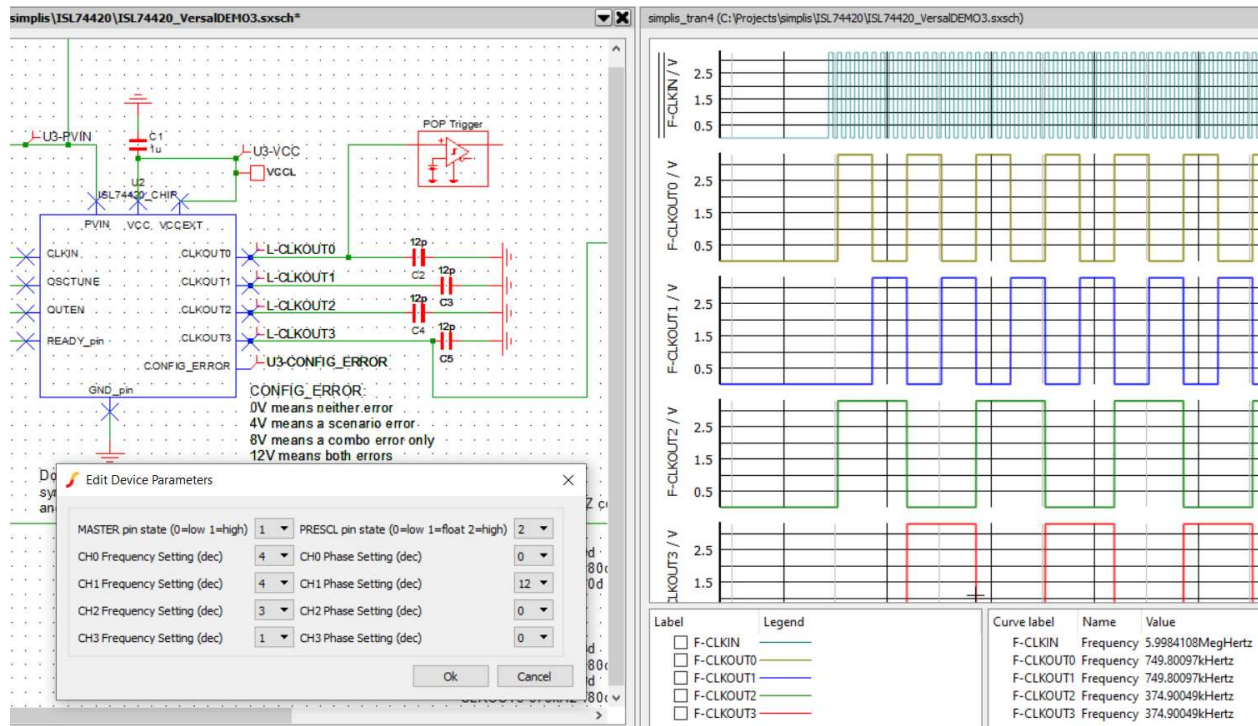


Figure 4: VERSALDEMO3 application: Follower settings and results

4. Operation: Frequency and Phase Option Selection

Options that would normally be selected through pin-strapping or I²C commands on the actual chip can instead be selected through an onscreen Menu on the iSim model. An example of this menu is shown in Figure 5.

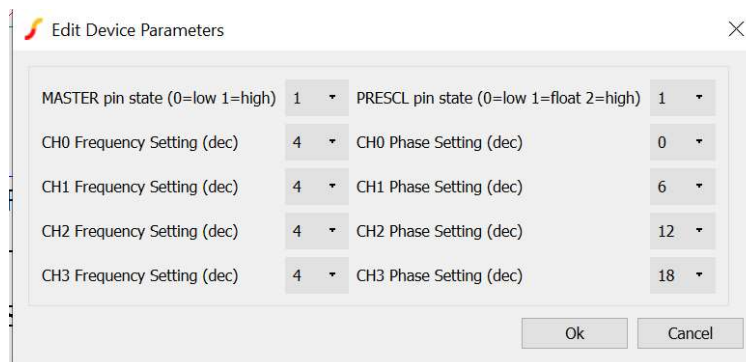


Figure 5: ISL74420 Simplis Popup Menu

The MASTER pin selection should be either 0 (for follower mode) or 1 (for leader mode). This affects the operation of the internal oscillator.

The PRESCAL pin selection should be 0, 1, or 2 to indicate 'low', 'float', or 'high', respectively. This affects the frequency division ratios of all four CLKOUT channels.

The "CHx Frequency..." settings are individual to each CLKOUT Channel. The Frequency selection can range from 0 to 13 (in decimal) which corresponds to the different rows of the Frequency Selection Table in the ISL74420x datasheets. When setting frequencies for the different CLKOUT channels, certain "Scenario" rules must be followed. These are noted in the datasheet and in Section 5.2 of this document.

The “CHx Phase...” settings are also individual to each CLKOUT channel. The Phase selection can range from 0 to 23 (in decimal) which corresponds to the different phase delay options in the Phase Selection Table in the ISL74420x datasheets. When setting phases for the different CLKOUT channels, the “Scenario” rules must be followed. In addition, frequency options 0, 1, 2, and 3 do not support all phase options. These are noted in the datasheet and in Section 5.1 of this document.

5. Operation: Configuration Errors

The model's CONFIG_ERROR output pin is not a real pin on the device. It is a diagnostic tool to help the user of the model figure out why their configuration is incorrect. When this pin is high, the selected configuration is not supported by the model or the actual part.

- If the CONFIG_ERROR pin equals 0V, there is no configuration error
- If the CONFIG_ERROR pin equals 4V, there is a “Scenario Error”
- If the CONFIG_ERROR pin equals 8V, there is a “Combination Error”
- If the CONFIG_ERROR pin equals 12V, there are both “Scenario” and “Combination” errors.

5.1 Unsupported Frequency and Phase Combinations

A “Combination error” means that the selected phase option for one of the CLKOUT channels is not supported by that channel's frequency option. This error can only occur with Frequency options 0, 1, 2, or 3. Frequency options 4-13 support all 24 phase options.

Frequency Option	Supported Phase Options (°)	Supported Phase Options (dec)
0	0°	0
1	0°, 180°	0, 12
2	0°, 90°, 180°, 270°	0, 6, 12, 18
3	0°, 60°, 120°, 180°, 240°, 300°	0, 4, 8, 12, 16, 20

Table 1: Frequency Options with a Limited Phase Selection

The model and part will both respond to this error by defaulting to 0° phase delay for the affected channel.

5.2 Scenario Errors

Scenario Errors are more complicated to describe and debug. So, if the configuration does not fall into one of these specific configuration scenarios, the model will raise the CONFIG_ERROR pin by 4V and will not provide output clocks. The actual part does not have this level of protection. If the actual part is presented with an invalid configuration, it will try to provide clocks, but the configuration is unsupported by the internal logic so the clocks may not be the correct.

Please refer to the part's datasheet for the most recent description of Scenarios.

- Scenario 1 – All four outputs are at the same frequency
 - The phase configurations for each of the four output clocks are user configurable.
- Scenario 2 – Three outputs have the same frequency, 1 output at a different frequency
 - The three outputs with the same frequency must be on outputs CLKOUT0, CLKOUT1, and CLKOUT2.
 - The phase configurations for CLKOUT0, 1, and 2 are user configurable.

- The different frequency must be on CLKOUT3.
 - The phase configuration for CLKOUT3 is ignored and defaults to 0°.
- Scenario 3 – Two outputs have the same frequency, the other two outputs are at a different but same frequency (such as, two outputs at 500kHz, two other outputs at 333kHz)
 - One pair of same frequencies must be on CLKOUT0 and CLKOUT1.
 - The other pair of frequencies must be on CLKOUT2 and CLKOUT3.
 - The phase relationship of CLKOUT0 and CLKOUT1 is user configurable.
 - The phase relationship of CLKOUT2 and CLKOUT3 is user configurable.
 - The phase relationship between outputs of different frequencies (such as, CLKOUT0 and CLKOUT3) is the result of frequencies selected.
- Scenario 4 – Two outputs have the same frequency, the other two outputs are at two different frequencies (there are three total different frequencies output)
 - The pair of same frequencies must be on CLKOUT0 and CLKOUT1.
 - The phase configurations for CLKOUT0 and CLKOUT1 are selectable.
 - The two different frequencies must be on CLKOUT2 and CLKOUT3
 - The phase configuration for CLKOUT2 and CLKOUT3 are ignored and default to 0°.
- Scenario 5 – All four outputs are at different frequencies
 - The frequencies can be in any order on any CLKOUTx channel.
 - The phase configuration for all CLKOUTx is ignored and defaults to 0°.

6. Operation: OUTEN and READY

The READY pin is an open-drain output that pulls low while the part is initializing. The model matches the part's performance by holding READY low for approximately 2ms after VCC and PVIN are both okay. Upon releasing the READY pin, the model is ready to output clock signals.

As is typical for open-drain outputs on CMOS ICs, the part cannot pull READY low if VCC is below 1.2V. This function is modeled, and can be observed by providing a resistive pullup to the READY pin from a DC source instead of the part's own VCC.

The OUTEN pin is a CMOS input that can be used to enable and disable the output clocks. This is ANDed with an internal READY signal so that both must be OK for clocks to begin. Any rising edge on OUTEN will reset the phasing of clocks to begin at 0d. Clocks with a phase higher than 180° will remain off until it is their proper time to have a rising edge.

7. Operation: OSCTUNE and Oscillator Tolerance

The core oscillator frequency in the model can be tuned with an external OSCTUNE resistor the same way the real part is tuned. The performance matches the ISL74420M datasheet Table 3 "OSCTUNE Resistor and Nominal Frequency".

Table 3. OSCTUNE Resistor and Nominal Frequency

OSCTUNE Resistor (kΩ)	Oscillator Frequency (MHz)	Tuning Range (%)
8.2	52.8	110
10	50.4	105
12.7	48	100
17.8	45.6	95
26.7	43.6	91

Figure 6: Table 3 excerpt from the ISL74420M datasheet

In addition to the external tuning, there is a method to simulate the oscillator tolerance by adjusting the part internally. The intent is so the user can perform “Worst Case Analysis” and reach the datasheet specification oscillator frequency limits.

This feature is only available to users of the unencrypted model in full Simplis. Contact a Renesas representative if you need access to the model that supports this internal tuning ability.

Clock Output Timing							
Internal Oscillator Nominal Frequency	InternalOsc_Nom	OSCTUNE = 12.7kΩ, PVIN = VCC = [3V, 3.6V] VCC regulating and PVIN = [5V, 12V, 18V]	-55°C	47.5	49.92	51.5	MHz
			+25°C	46.50	48.22	49.25	
			+125°C	45.25	47.59	49.0	
			+25°C (Post Rad)	46.25	47.72	49.25	
Internal Oscillator Minimum Frequency	InternalOsc_Min	PVIN = [5V, 12V, 18V], OSCTUNE = 26.7kΩ	-55 to +125°C	41.0	43.6	46.2	MHz
Internal Oscillator Minimum Frequency	InternalOsc_Min	PVIN = VCC = [3V, 3.6V], OSCTUNE = 26.7kΩ	-55 to +125°C	41.0	43.6	46.2	MHz
Internal Oscillator Maximum Frequency	InternalOsc_Max	PVIN = [5V, 12V, 18V], OSCTUNE = 8.2kΩ	-55 to +125°C	49.5	52.8	56.5	MHz
Internal Oscillator Maximum Frequency	InternalOsc_Max	PVIN = VCC = [3V, 3.6V], OSCTUNE = 8.2kΩ	-55 to +125°C	48.5	52.5	56.5	MHz

Figure 7: Internal Oscillator Specification Table from ISL74420M datasheet

The adjustment is done by changing a resistor inside the ISL74420 Simplis Model.

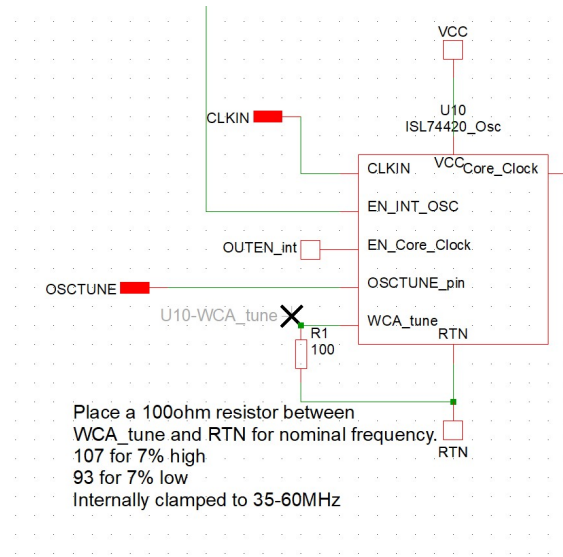


Figure 8: Simplis Model WCA tuning resistor

External OSCTUNE resistor (Ω)	Target Frequency (MHz)	WCA Resistor (Ω)	Model Frequency (MHz)
8.2k	56.5	$100 \times (56.5/52.8) = 107$	56.48
	52.8	100	52.78
	48.5	$100 \times (48.5/52.8) = 91.9$	48.5
12.7k	51.5	$100 \times (51.5/48) = 107.3$	51.49
	48	100	47.99
	45.25	$100 \times (45.25/48) = 94.3$	45.25
26.7k	46.2	$100 \times (46.2/43.6) = 106$	46.2
	43.6	100	43.6
	41.0	$100 \times (41/43.6) = 94$	40.98

This table summarizes the results of simulation using the expected WCA resistor. Further tuning could be done to arrive at the “perfect” WCA resistor for each target frequency.

8. Absolute Maximum Ratings

The model checks each pin against its abs max rating and will raise the “CONFIG_ERROR” pin by 1V to indicate an error. It also stops operating when an abs max error is present.

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
PVIN	GND - 0.3	GND + 20	V
PVIN ^[1]	GND - 0.3	GND + 20	V
VCC, VCCEXT	GND - 0.3	GND + 6.5	V
VCC ^[1] , VCCEXT ^[1]	GND - 0.3	GND + 6.5	V
OSCTUNE	GND - 0.3	VCC	V
CLKIN	GND - 0.3	GND + 6.5	V
CLKOUTx	GND - 0.3	VCCEXT + 0.3; GND + 6.5	V
CHx PH[x], CHx FREQ[x]	GND - 0.3	GND + 6.5	V
SDA, SCL	GND - 0.3	GND + 6.5	V
READY	GND - 0.3	GND + 6.5	V
MASTER, OUTEN	GND - 0.3	GND + 6.5	V
Junction Temperature	-55	+150	°C
Storage Temperature	-65	+150	°C
Human Body Model (Tested per JS-001-2023)	-	2.0	kV
Charged Device Model (Tested per JS-002-2022)	-	750	V
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	±100	mA

1. Tested under a heavy ion environment at LET = 46MeV·cm²/mg at +125°C (T_C) for SEB.

Figure 9: ISL74420M datasheet Abs Max ratings

9. Revision History

Revision	Date	Description
1.00	July 28, 2025	Initial release.